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Page 1 of 54

Urgent

Confidential

Date: October 28, 2004

To:
Examiner:
Alexander O. Williams
USPTO

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Art Unit:
2826

From:
Jay P. Beale

Fax:
703-633-3303

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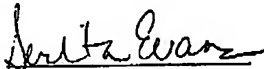
Subject: A Process of Vertically Stacking Multiple Wafers Supporting Different...
Application No.: 10/066,643; Inventor: Kellar et. al.
Filed: 2/6/2002 Docket No. 042390.P12752

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Serita Evans

Date: 10/28/04



Included in this transmission:
Fax Cover Sheet (1 page)
RCE Transmittal - PTO/SB30 (1 page submitted in duplicate)
Preliminary Amendment (3 pages)
Figures 1A-B, 2-5 and 6A-B (4 pages)
Information Disclosure Statement w/ PTO-1449 (5 pages)
One non-US reference (15 pages)
One non-published application (24 pages)

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OCT 28 2004

Application No. : 10/066,643
Applicant : Kellar, et al.
Filed : February 6, 2002
TC/AU : 2826
Examiner : Williams, Alexander O.
Docket No. : 42390.P12752
Customer No. : 08791

Confirmation No.: 4503

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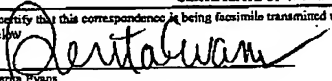
Preliminary Amendment

Examiner,

This Preliminary Amendment accompanies the filing of a Request for Continuing
Examination in this application.

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

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By:  Serina Evans	Date: October 28, 2004

Preliminary Amendment

Application 10/066,643
Attorney Docket: 042390.P12752

Amendments to the Specification

Please insert the following paragraph before the first paragraph in the specification:

This application is related to the following patents and pending patent applications, which are assigned to the assignee of this application: US Patent 6,661,085, filed on February 6, 2002 and issued on December 9, 2003; US Patent Application serial number 10/066,645, filed on February 6, 2002; US Patent 6,762,076, filed on February 20, 2002 and issued on July 13, 2004; US Patent Application serial number 10/613,006, filed on July 7, 2003; US Patent Application serial number 10/695,328, filed on October 27, 2003; and US Patent Application serial number 10/855,032, filed on May 26, 2004.

219.40232X00
LID#: P12070**CLAIMS:**

1 1. A method of vertically stacking wafers, comprising:
2 selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;
3 bonding the adjacent wafers, via respective metallic lines on opposing surfaces of the adjacent wafers, to
4 establish electrical connections between active devices on vertically stacked wafers; and
5 forming one or more vias to establish electrical connections between the active devices on the vertically
6 stacked wafers and an external interconnect.

1 2. The method as claimed in claim 1, wherein each via is formed by:
2 selectively etching the top wafer to form a via;
3 depositing an oxide layer to insulate a sidewall of the via;
4 forming a barrier/seed layer in the via; and
5 depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection
6 between active devices on the vertically stacked wafers and the external interconnect.

1 3. The method as claimed in claim 1, wherein the metallic lines are Copper (Cu) lines deposited to
2 serve as electrical contacts between active devices on the vertically stacked wafers.

1 4. The method as claimed in claim 2, wherein the conduction metal deposited in the via is copper
2 (Cu) or a Cu alloy.

1 5. The method as claimed in claim 2, wherein the barrier/seed layer contains a barrier layer deposited
2 in the via, and a copper (Cu) seed layer deposited in the trench overlying the barrier layer.

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LID#: P12070

6. The method as claimed in claim 5, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

7. The method as claimed in claim 1, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

8. The method as claimed in claim 1, wherein the vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

9. The method as claimed in claim 1, wherein each via is formed by a dual damascene process comprised of:

- selectively etching the top wafer to form an upper trench section of a via;
- depositing an oxide layer to insulate a sidewall of the upper trench section of the via;
- selectively etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;
- depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and
- depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and an external interconnect.

10. The method as claimed in claim 9, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier

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LiD#: P12070

5 layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the
6 via.

1 11. The method as claimed in claim 1, wherein the vias are formed during a Shallow Trench Isolation
2 (STI) process in the top wafer before the adjacent wafers are bonded, via the respective metallic lines deposited on
3 opposing surfaces of the adjacent wafers.

1 12. A method of forming vertically stacked wafers, comprising:
2 depositing a plurality of metallic lines on opposing surfaces of top and bottom wafers;
3 forming a conductive plug;
4 bonding the adjacent wafers, via respective metallic lines, to form vertically stacked wafers; and
5 forming at least one via on the top wafer to establish electrical connections between the active devices on
6 the vertically stacked wafers and an external interconnect, by selectively etching through the top wafer until stopped
7 by the conductive plug, depositing an oxide layer to insulate a sidewall of the via, depositing a barrier/seed layer on
8 the bottom of the via, and filling the via with a conduction metal to serve as electrical connections between active
9 devices on the vertically stacked wafers and the external interconnect.

1 13. The method as claimed in claim 12, wherein the metallic lines are Copper (Cu) lines deposited to
2 serve as electrical contacts between active devices on the vertically stacked wafers.

1 14. The method as claimed in claim 12, wherein the conduction metal deposited in the via is copper
2 (Cu) or a Cu alloy.

1 15. The method as claimed in claim 12, wherein the barrier/seed layer contains a barrier layer
2 deposited in the via, and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

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LID#: P12070

1 16. The method as claimed in claim 15, wherein the barrier layer is comprised of a material selected
2 from one of the group including tantalum, titanium, and tungsten, and the Cu seed layer is comprised of a few layers
3 of copper (Cu) atoms deposited on the barrier layer by chemical vapor deposition (CVD) process.

1 17. The method as claimed in claim 12, further comprising dummy vias arranged on opposing
2 surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary
3 structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

1 18. The method as claimed in claim 12, wherein the via is formed tapered from the top to the bottom
2 via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

1 19. A three-dimensional (3-D) vertically stacked wafer system, comprising:
2 a first wafer including an active region to support one or more integrated circuit (IC) devices;
3 a second wafer including an active region to support one or more integrated circuit (IC) devices;
4 metallic lines deposited on opposing surfaces of the first and second wafers at designated areas to establish
5 metal bonding between the first and second wafers in a stack and provide electrical connections between active IC
6 devices on the first and second wafers in the stack; and
7 one or more vias formed, via the active region of the first wafer, to serve as electrical connections between
8 the active IC devices on the first and second wafers in the stack and an external interconnect.

1 20. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 19, wherein the
2 metallic lines include Copper (Cu) lines deposited on opposing surfaces of the first and second wafers to serve as
3 electrical contacts between active IC devices on the first and second wafers.

1 21. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each
2 via is formed by:

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3 selectively etching the first wafer to form a via;
4 depositing an oxide layer to insulate a sidewall of the via;
5 forming a barrier/seed layer in the via; and
6 depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection
7 between active IC devices on the vertically stacked wafers and the external interconnect.

1 22. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 21, wherein the
2 conduction metal deposited in the via is copper (Cu) or a Cu alloy, and the barrier/seed layer includes a barrier layer
3 deposited in the via overlying the oxide layer and a copper (Cu) seed layer deposited in the via overlying the barrier
4 layer.

1 23. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 22, wherein the
2 barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride
3 (Ta₂N₃), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited
4 on the barrier layer by chemical vapor deposition (CVD) process.

1 24. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each
2 via is formed by a dual damascene process comprised of:
3 selectively etching the top wafer to form an upper trench section of the via;
4 depositing an oxide layer to insulate a sidewall of the upper trench section of the via;
5 etching the oxide layer in the upper trench section to form a lower trench section of the via;
6 depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and
7 depositing a conduction metal on the barrier/seed layer for providing an electrical connection between
8 active devices on the vertically stacked wafers and the external interconnect.

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1 25. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 24, wherein the
2 barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum
3 (Ta), tantalum nitride (Ta₂N₃), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the
4 oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper
5 (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the
6 lower trench section of the via.

1 26. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein the
2 vias are formed during a Shallow Trench Isolation (STI) process in the first wafer before the first and second wafers
3 are bonded, via the respective metallic lines deposited on opposing surfaces of the first and second wafers.

1 27. A three-dimensional (3-D) vertically stacked wafer system, comprising:
2 a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing
3 surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and
4 provide electrical connections between active IC devices on the adjacent wafers;
5 a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing
6 surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and
7 provide electrical connections between active IC devices on the adjacent wafers; and
8 one or more vias formed on opposing surfaces of the first stack of wafers and the second stack of adjacent
9 wafers to serve as electrical connections between the active IC devices on the first and second stacks of wafers and
10 an external interconnect.

1 28. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the
2 metallic lines include Copper (Cu) lines deposited on opposing surfaces of the adjacent wafers in the first and
3 second stacks of wafers to serve as electrical contacts between active IC devices on the first and second stacks of
4 wafers.

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LID#: P12070

1 29. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, further
2 comprising dummy vias arranged on opposing surfaces of the first and second stacks of adjacent wafers to increase
3 the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits
4 for the active IC devices on vertically stacked wafers.

1 30. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the
2 vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding
3 in the first and second stacks of adjacent wafers.

1 31. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein each
2 via is formed by a dual damascene process comprised of:
3 selectively etching the top wafer to form an upper trench section of a via;
4 depositing an oxide layer to insulate a sidewall of the upper trench section of the via;
5 etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;
6 depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and
7 depositing a conduction metal on the barrier/seed layer for providing an electrical connection between
8 active IC devices on the vertically stacked wafers and the external interconnect.

1 32. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 31, wherein the
2 barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum
3 (Ta), tantalum (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide
4 layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu)
5 deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the
6 lower trench section of the via.

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LID#: P120701
2 **ABSTRACT OF DISCLOSURE**

3 A method of vertically stacking wafers is provided to form three-dimensional (3D) wafer stack. Such
4 method comprising: selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;
5 bonding the adjacent wafers, via the metallic lines, to establish electrical connections between active devices on
6 vertically stacked wafers; and forming one or more vias to establish electrical connections between the active
7 devices on the vertically stacked wafers and an external interconnect. Metal bonding areas on opposing surfaces of
8 the adjacent wafers can be increased by using one or more dummy vias, tapered vias, or incorporating an existing
copper (Cu) dual damascene process.

Preliminary Amendment

Application 10/088,643
Attorney Docket: 042390.P12752

Remarks

Applicants respectfully request entry of the amendments to the specification offered herein. Applicants have also taken this opportunity to present formal drawings (Figs. 1A-B, 2-5 and 6A-B). If the Examiner has any questions, Examiner is invited to contact the undersigned at (703) 633-0927. If any fee insufficiency or overpayment is found, please charge the insufficiency or credit the overpayment to Deposit Account 50-0221.

Respectfully submitted,

Dated:

28 Oct 04



Jay Beale,
Intel Corp.
Reg. No. 50,901

c/o Intel Americas
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Chantilly, VA 20151
(703) 633-0927

PTO/SB/30 (09-03)

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Request for Continued Examination (RCE) Transmittal

Address to:
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P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/066,643
Filing Date	February 6, 2002
First Named Inventor	Scott A. Keller
Art Unit	2826
Examiner Name	Alexander O. Williams
Attorney Docket Number	042390.P12752

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1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

ii. ☐ Other _____

b. ☒ Enclosed

i. ☒ Amendment/Reply

iii. ☒ Information Disclosure Statement (IDS)

ii. ☐ Affidavit(s)/ Declaration(s)

iv. ☒ Other Formal Docs: Figs. 1A-B, 2-5 and 6A-B

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(f) required)

b. ☐ Other _____

3. Fees

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed. The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0221

a. ☒ RCE fee required under 37 CFR 1.17(e)

ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

iii. ☐ Other _____

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Name (Print/Type)	Jay Beale	Registration No. (Attorney/Agent)	50,901
Signature		Date	2/20/04

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Name (Print/Type)	Serita Evans	Date	10/28/04
Signature			

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Alexandria, VA 22313-1450

Application Number	10/086,843
Filing Date	February 6, 2002
First Named Inventor	Scott A. Kellar
Art Unit	2826
Examiner Name	Alexander O. Williams
Attorney Docket Number	042390.P12752

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a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

ii. ☐ Other _____

b. ☒ Enclosed

i. ☒ Amendment/Reply

iii. ☒ Information Disclosure Statement (IDS)

ii. ☐ Affidavit(s)/ Declaration(s)

iv. ☒ Other Formal Drawings: Figs. 1A-B, 2-5 and 6A-B

2. Miscellaneous

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b. ☐ Other _____

3. Fees

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The Director is hereby authorized to charge the following fees, or credit any overpayments, to

a. ☒ Deposit Account No. 50-0221

i. ☒ RCE fee required under 37 CFR 1.17(e)

ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

iii. ☐ Other _____

b. ☐ Check in the amount of \$ _____ enclosed

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Jay Beale	Registration No. (Attorney/Agent)	50,901
Signature		Date	2/28/04

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Name (Print/Type)	Serita Evans	Date	10/28/04
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/066,643	Confirmation No.:	4603
Applicant	:	Kellar, et al.		
Filed	:	February 6, 2002		
TC/AU	:	2826		
Examiner	:	Williams, Alexander O.		
Docket No.	:	42390.P12752		
Customer No.	:	08791		

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement under 37 C.F.R. 1.97

Examiner,

Please consider the documents cited in the accompanying Information Disclosure Statement form during the examination of the above-referenced patent application. It is respectfully requested that the IDS form be initiated by the Examiner to indicate such consideration, and that a copy of the initiated form be returned to the applicants. This IDS is being submitted before the mailing of a first action on the merits.

The documents listed in the IDS are cited in the following related patents and pending patent applications, which are assigned to the assignee of the present application: US Patent 6,661,085, filed on February 6, 2002 and issued on December 9, 2003; US Patent Application serial number 10/066,645, filed on February 6, 2002; US Patent 6,762,076, filed on February 20, 2002 and issued on July 13, 2004; US Patent Application serial number 10/613,006, filed on July 7, 2003; US Patent Application serial number 10/695,328, filed on October 27, 2003; and US Patent Application serial number 10/855,032, filed on May 26, 2004.

IDS


Application 10/066,643
Attorney Docket: 042390.P12752

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Respectfully submitted,

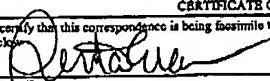
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28 Oct, '04



Jay Beale,
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			Application Number	10/066,643	
Sheet	1	of	3	Filing Date	February 6, 2002
				First Named Inventor	Kellar
				Art Unit	2826
				Examiner Name	Williams, Alexander O.
				Attorney Docket Number	42390.P12752

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Examiner Initials*	Cite No.†	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code* (if known)				
		US- 4,689,113		8/25/1987	Balasubramanyam, et	
		US- 6,559,042		5/8/2003	Barth, et al.	
		US- 5,241,450		8/31/1993	Barnhardt, et al.	
		US- 5,880,010		3/9/1999	Davidson	
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		US- 5,827,106		6/6/1997	Hau	
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		EP0293459B1	7/22/1992	Carlomagno		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/066,643
		Filing Date	February 5, 2002
		First Named Inventor	Kellar
		Art Unit	2828
		Examiner Name	Williams, Alexander O.
Sheet 2 of 3	Attorney Docket Number	42390.P12752	

U.S. PATENT DOCUMENTS						
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		Number-Kind Code‡ (§ 1.702)				
		US- 5,473,197		12/5/1995	Idaka, et al.	
		US- 6,681,085		12/9/2003	Kellar, et al.	
		US- 20040142540	A1	7/22/2004	Kellar, et al.	
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